

United States Patent and Trademark Office

UNITED STATES DEPARTMENT OF COMMERCE United States Patent and Trademark Office Address: COMMISSIONER FOR PATENTS P.O. Box 1450 Alexandria, Virginia 22313-1450 www.uspto.gov

CONFIRMATION NO. APPLICATION NO. FILING DATE FIRST NAMED INVENTOR ATTORNEY DOCKET NO. 10/517,327 12/09/2004 Roland Brandl AT02 0034 US 24738 . 7590 EXAMINER 11/01/2005 PHILIPS ELECTRONICS NORTH AMERICA CORPORATION PATEL, DHARTI HARIDAS INTELLECTUAL PROPERTY & STANDARDS ART UNIT PAPER NUMBER 1109 MCKAY DRIVE, M/S-41SJ SAN JOSE, CA 95131 2836

DATE MAILED: 11/01/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

	Application No.	Applicant(s)
	10/517,327	BRANDL, ROLAND
Office Action Summary	Examiner	Art Unit
	Dharti H. Patel	2836
The MAILING DATE of this communication appears on the cover sheet with the correspondence address Period for Reply		
A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION. - Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication. - If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely. - If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication. - Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).		
Status		
1) Responsive to communication(s) filed on 09 December 2004.		
	action is non-final.	
3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under <i>Ex parte Quayle</i> , 1935 C.D. 11, 453 O.G. 213.		
Disposition of Claims		
4) ☐ Claim(s) 1-4 is/are pending in the application. 4a) Of the above claim(s) is/are withdrawn from consideration. 5) ☐ Claim(s) is/are allowed. 6) ☐ Claim(s) 1-4 is/are rejected. 7) ☐ Claim(s) is/are objected to. 8) ☐ Claim(s) are subject to restriction and/or election requirement.		
Application Papers		
9) ☐ The specification is objected to by the Examiner. 10) ☑ The drawing(s) filed on <u>09 December 2004</u> is/are: a) ☑ accepted or b) ☐ objected to by the Examiner. Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a). Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d). 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.		
Priority under 35 U.S.C. § 119		
 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f). a) All b) Some * c) None of: 1. Certified copies of the priority documents have been received. 2. Certified copies of the priority documents have been received in Application No 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)). * See the attached detailed Office action for a list of the certified copies not received. 		
Attachment(s) 1) Notice of References Cited (PTO-892) 4) Interview Summary (PTO-413)		
 Notice of References Cited (PTO-892) Notice of Draftsperson's Patent Drawing Review (PTO-948) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 	Paper No(s)/Mail Da	

1.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1 and 3 are rejected under 35 U.S.C. 103(a) as being unpatentable over the acknowledged prior art, in view of Duvvury et al., Patent No. 5,493,133. With respect to claim 1, applicant's acknowledged prior art (Fig. 1) teaches a data carrier 1 that includes an integrated circuit 5 which comprises a first terminal 6 and a second terminal 7, wherein the two terminals are provided for connection with transmission means 2 of the data carrier 1 and an ESD protection circuit 8, which is connected between the two terminals 6 and 7 and which comprises a series connection 9 consisting of a first protection diode 10 and a protection stage 11, which protection stage 11 may be brought from a blocking state into a conductive state by exceeding a voltage threshold, and which comprises a second protection diode 12 connected in parallel with the series connection 9 and in opposition to the first protection diode 10 of the series connection 9, and a rectifier circuit 13, which is connected to the ESD protection circuit 8 and comprises a rectifier diode 14 connected in parallel with the ESD protection circuit 8 as disclosed in Specifications, Page 4, lines 9-18, 24-27, 32-33 and Fig.

Application/Control Number: 10/517,327

Art Unit: 2836

However, the prior art fails to teach or suggest a rectifier diode of the rectifier circuit takes the form of a Schottky diode with a parasitic p/n junction and wherein the Schottky diode with the parasitic p/n junction forms the second protection diode of the ESD protection circuit.

Duvvury et al. teaches protection devices for integrated circuits, protection devices having positive and negative stress pin voltages with respect to substrate operation requirements. The protection circuit comprises a silicon-controlled rectifier 60, which further comprises first diffused region, a well region and a third diffused region located in a substrate; and a Schottky diode 64 that is connected to said well region of a SCR 60 as disclosed in Col. 4, lines 38-40 and Col. 5, lines 10-11. The Schottky diode 64 is used for biasing the n-well region 44 so that non ESD event latchup may be prevented.

Both teachings are related by being integrated circuits having rectifiers for ESD protection. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Duvvury et al., which teaches a Schottky diode, into the integrated circuit for a data carrier of the applicant's acknowledged prior art because it is desirable to use a simple rectifier-filter circuit using Schottky-type diodes to have a lower forward voltage drop across the rectifier diodes when conducting, which increases the rectification efficiency.

With respect to claim 3, applicant's acknowledged prior art (Fig. 1) teaches a data carrier 1 that includes an integrated circuit 5 which comprises a

Art Unit: 2836

first terminal 6 and a second terminal 7, wherein the two terminals are provided for connection with transmission means 2 of the data carrier 1 and an ESD protection circuit 8, which is connected between the two terminals 6 and 7 and which comprises a series connection 9 consisting of a first protection diode 10 and a protection stage 11, which protection stage 11 may be brought from a blocking state into a conductive state by exceeding a voltage threshold, and which comprises a second protection diode 12 connected in parallel with the series connection 9 and in opposition to the first protection diode 10 of the series connection 9, and a rectifier circuit 13, which is connected to the ESD protection circuit 8 and comprises a rectifier diode 14 connected in parallel with the ESD protection circuit 8 as disclosed in Specifications, Page 4, lines 9-18, 24-27, 32-33 and Fig. 1. Claim 3 differs from claim 1 by having a data carrier for contactless communication with a communications station. The above mentioned data carrier may provide contactless communication when the transmission means is an antenna or transceiver. The admitted prior art does not specifically mention what the transmission means comprises. Furthermore, it would have been obvious to those skilled in the art at the time of the invention that the above mentioned data carrier may be provided for both contact and contactless communication in a data carrier to provide circuitry that incorporates a simple rectifier filer that increases rectification efficiency. The teachings of Duvvury et al. would apply to reject claim 3.

Application/Control Number: 10/517,327

Art Unit: 2836

2. Claims 2 and 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over applicant's prior art in view of Duvvury et al. as applied to claims 1 and 3 above, and further in view of Ellis, Patent No. 5,550,728. With respect to claims 2 and 4, applicant's prior art as modified by Duvvury is silent as to the rectifier circuit taking the form of a voltage doubler circuit. Ellis teaches a charge pump converter structure 100 that takes the form of voltage doubler circuit as disclosed in Fig. 3A. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Ellis, which teaches a voltage doubler circuit, into the integrated circuit for a data carrier taught by applicant's prior art as modified by Duvvury et al. to have a lower forward voltage drop in rectifier circuits, which increases the rectification efficiency; and to provide the best performance in the high frequency bands.

3. Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dharti H. Patel whose telephone number is 571-272-8659. The examiner can normally be reached on 8:30am - 5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Brian Sircus can be reached on 571-272-2800, Ext. 36. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information

Application/Control Number: 10/517,327 Page 6

Art Unit: 2836

for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DHP 10/24/2005

PHUONGT.VU